REMARKS

This is a full and timely response to the outstanding Office action mailed October 6, 2003. The examiner is thanked for the thorough examination of this application and for allowing claims 1, 2, 7-10, 13, 21-24 and 29-30. Upon entry of the amendments in this response claims 1-30 remain pending. More specifically, claims 3 and 14 are amended. These amendments are specifically described hereinafter. It is believed that the foregoing amendments add no new matter to the present application.

I. Present Status of Patent Application

Claims 3, 4, 6 and 27 are rejected under 35 U.S.C. 102(e) as allegedly anticipated by Bedingfield et al. (U.S. Patent No. 6,236,675). Claim 5 is rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Bedingfield et al. (U.S. Patent No. 6,236,675). Claims 11, 12, 14-20, 25, 26 and 28 are rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Aslanis et al. (previously cited in Office Action 7/28/03).

II. Summary of Present Application

The present application is directed to systems and methods for reducing the pilot tone phase interference at a receiver in a DMT communication system. One embodiment of the system can be implemented as follows. Providing a DMT receiver in communication with an analog to digital converter (ADC) in the downstream data path. The ADC in further communication with a phase locked-loop (PLL) which completes a feedback loop by correcting the timing in the ADC.

In one embodiment, a carefully chosen scrambler seed is used in generating the C-REVERB, C-SEGUE, and C-MEDLEY signals in the transmitter such that the phase offsets in the pilot tone are minimized.

In another embodiment, a state machine, already needed in DSL modems, controls the base timing recovery system. The state machine may be configured to recognize the far-end signal and to compensate for the pilot tone phase offset accordingly.

In another embodiment, a symbol synchronizer, also needed in DMT DSL modems, rather than a state machine, may be used to control the base timing recovery system. The symbol synchronizer may be configured to receive the far-end signal and to recognize when the cyclic prefix is present. The symbol synchronizer is further configured to squelch the cyclic prefix in the far-end signal from the input to the PLL.

In another embodiment an equalizer becomes part of the timing recovery system. The channel shortening time-domain equalizer may be configured to confine the cyclic prefix within the 32-sample period and to feeds its output to the timing recovery PLL with the cyclic prefix squelched.

Another embodiment further integrates a DFT in the timing recovery system to estimate the pilot tone phase error in the frequency domain. The pilot tone phase error is applied to a modified PLL (the band-pass filter and local oscillator are no longer required having been replaced by the DFT).

IV. Rejections Under 35 U.S.C. §102(e)

A. Claims 3, 4, and 6

The Office Action rejects claims 3, 4, and 6 under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,236,675 to Bedingfield et al. For the reasons set forth below, Applicants respectfully traverse the rejections.

For a proper rejection of a claim under 35 U.S.C. §102, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 7 U.S.P.Q.2d 1129 (Fed. Cir. 1988).

Applicants respectfully submit that independent claim 3 as amended is allowable for at least the reason that *Bedingfield* does not disclose, teach, or suggest at least the step of applying the frequency correction signal ***from the PLL to the ADC*** to modify the sampling time of the ADC. Instead, *Bedingfield* discloses a system where the output of the PLL (which contains an oscillator) is fed to either a noise compensator or an 8 bit DAC, then to a low pass filter and to a VCXO (another oscillator) before sending a signal to adjust the sampling time of the ADC.

Unless *Bedingfield* demonstrates sending an error signal directly from the PLL to the ADC, it cannot anticipate claim 3. Notwithstanding, the undersigned has reviewed the entirety of the *Bedingfield* patent and has failed to identify any such teaching anywhere within this reference. Therefore, *Bedingfield* does not anticipate claim 3 and the rejection should be withdrawn.

Because independent claim 3 as amended is allowable over the prior art of record, dependent claims 4 and 6 (which depend from independent claim 3) are allowable as a matter of law for at least the reason that dependent claims 4 and 6 contain all the steps/features of independent claim 3. *See Minnesota Mining and Manufacturing Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002) *Jeneric/Pentron, Inc. v. Dillon Co.*, 205 F.3d 1377, 54 U.S.P.Q.2d 1086 (Fed. Cir. 2000); *Wahpeton Canvas Co. v. Frontier Inc.*, 870 F.2d 1546, 10 U.S.P.Q.2d 1201 (Fed. Cir. 1989). Therefore, since dependent claims 4 and 6 are patentable over *Bedingfield*, the rejection to claims 4 and 6 should be withdrawn and the claims allowed.

Additionally and notwithstanding the foregoing reasons for allowability of independent claim 3, dependent claims 4 and 6 recite further features and/or combinations of features, as are apparent by examination of the claims themselves, that are patently distinct from the prior art of record. Hence, dependent claims 4 and 6 are allowable for these additional reasons as well.

B. Claim 27

The Office Action rejects claims 27 under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,236,675 to Bedingfield *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §102, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 7 U.S.P.Q.2d 1129 (Fed. Cir. 1988).

Applicants respectfully submit that independent claim 27 is allowable for at least the reason that *Bedingfield* does not disclose, teach, or suggest at least a means for applying the phase error to a phase locked-loop to generate an output signal ***responsive to when the cyclic prefix is not present in the digital signal.*** The Examiner cites Fig. 5 and column 5, lines 36-40 as demonstrating a means for applying the phase error responsive to when the cyclic prefix is not

present in the digital signal. Column 5, lines 36-40 recites, "The signal is then supplied on line 78 to phase locked loop 87 which scales and integrates the signal to determine any static frequency offset. The phase error and frequency offset are scaled and then added as is known in the art." This does not disclose anything concerning the presence of the cyclic prefix in the digital signal and particularly does not disclose applying the phase error responsive to when the cyclic prefix is absent. Notwithstanding, the undersigned has reviewed the entirety of the *Bedingfield* patent and has failed to identify any such teaching anywhere within this reference. Therefore, *Bedingfield* does not anticipate claim 27 and the rejection should be withdrawn.

V. Rejections Under 35 U.S.C. §103(a)

A. Claim 5

The Office Action rejects claim 5 under 35 U.S.C. §103(a) as allegedly unpatentable over Bedingfield *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

Because independent claim 3 is allowable over the prior art of record, dependent claim 5 (which depends from independent claim 3) is allowable as a matter of law for at least the reason that dependent claim 5 contains all the steps/features of independent claim 3. *See Minnesota Mining and Manufacturing Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002) *Jeneric/Pentron, Inc. v. Dillon Co.*, 205 F.3d 1377, 54 U.S.P.Q.2d 1086 (Fed. Cir. 2000); *Wahpeton Canvas Co. v. Frontier Inc.*, 870 F.2d 1546, 10 U.S.P.Q.2d 1201 (Fed. Cir. 1989). Therefore, the rejection to claim 5 should be withdrawn and the claim allowed.

Additionally and notwithstanding the foregoing reasons for allowability of independent claim 3, dependent claim 5 recites further features and/or combinations of features, as are apparent by examination of the claim itself, that are patently distinct from the prior art of record. Hence, dependent claim 5 is allowable for these additional reasons as well.

B. Claims 11 and 12

The Office Action rejects claim 11 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 11 is allowable for at least the reason that *Aslanis* does not disclose, teach, or suggest at least the step of applying the estimated phase error to the input of a ***phase locked-loop*** to create a frequency correction signal. *Aslanis* does not disclose a PLL for creating the error signal, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to create the frequency correction signal. Notwithstanding, the undersigned has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach, or suggest, either implicitly or explicitly, all the elements of claim 11 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 11 is allowable for these additional reasons as well.

Because independent claim 11 is allowable over the prior art of record, dependent claim 12 (which depends from independent claim 1) is allowable as a matter of law for at least the reason that dependent claim 12 contains all the steps/features of independent claim 11. *See Minnesota Mining and Manufacturing Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002) *Jeneric/Pentron, Inc. v. Dillon Co.*, 205 F.3d 1377, 54 U.S.P.Q.2d 1086 (Fed. Cir. 2000); *Wahpeton Canvas Co. v. Frontier Inc.*, 870 F.2d 1546, 10 U.S.P.Q.2d 1201 (Fed. Cir. 1989). Therefore, the rejection to claim 12 should be withdrawn and the claim allowed.

Additionally and notwithstanding the foregoing reasons for allowability of independent claim 11, dependent claim 12 recites further features and/or combinations of features, as are apparent by examination of the claim itself, that are patently distinct from the prior art of record. Hence, claim 12 is allowable for these additional reasons as well.

C. Claims 14 and 15

The Office Action rejects claim 14 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 14 as amended is allowable for at least the reason that *Aslanis* does not disclose, teach, or suggest at least an apparatus wherein a signal is sent to a ***phase locked-loop*** to compensate for the offset in phase error. *Aslanis* does not disclose a PLL for creating the error signal, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to compensate for the offset. Notwithstanding, the undersigned has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach or suggest, either implicitly or explicitly, all the elements of claim 14 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 14 is allowable for these additional reasons as well.

Because independent claim 14 is allowable over the prior art of record, dependent claim 15 (which depends from independent claim 14) is allowable as a matter of law for at least the reason that dependent claim 15 contains all the steps/features of independent claim 14. *See Minnesota Mining and Manufacturing Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir.

2002) *Jeneric/Pentron, Inc. v. Dillon Co.*, 205 F.3d 1377, 54 U.S.P.Q.2d 1086 (Fed. Cir. 2000); *Wahpeton Canvas Co. v. Frontier Inc.*, 870 F.2d 1546, 10 U.S.P.Q.2d 1201 (Fed. Cir. 1989). Therefore, the rejection to claim 15 should be withdrawn and the claim allowed.

Additionally and notwithstanding the foregoing reasons for allowability of independent claim 14, dependent claim 15 recites further features and/or combinations of features, as are apparent by examination of the claim itself, that are patently distinct from the prior art of record. Hence, claim 15 is allowable for these additional reasons as well.

D. Claim 16

The Office Action rejects claim 16 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 16 is allowable for at least the reason that *Aslanis* does not disclose, teach, or suggest at least an apparatus wherein a ***phase locked-loop*** is used. *Aslanis* does not disclose a PLL for adjusting the sampling rate of the ADC, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to adjust the sampling rate. Notwithstanding, the undersigned has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach or suggest, either implicitly or explicitly, all the elements of claim 16 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 16 is allowable for these additional reasons as well.

E. Claim 18

The Office Action rejects claim 18 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 18 is allowable for at least the reason that *Aslanis* does not disclose, teach, or suggest at least an apparatus wherein a ***phase locked loop*** is used to accept an error signal to adjust the sampling time of the ADC. *Aslanis* does not disclose a PLL for adjusting the sampling rate of the ADC, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to adjust the sampling rate. Notwithstanding, the undersigned has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach or suggest, either implicitly or explicitly, all the elements of claim 18 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 18 is allowable for these additional reasons as well.

F. Claim 19

The Office Action rejects claim 19 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 19 is allowable for at least the

reason that *Aslanis* do not disclose, teach, or suggest at least an apparatus wherein a ***phase locked loop*** is used to accept an error signal to adjust the sampling time of the ADC. *Aslanis* does not disclose a PLL for adjusting the sampling rate of the ADC, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to adjust the sampling rate. Notwithstanding, the undersigned has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach or suggest, either implicitly or explicitly, all the elements of claim 19 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 19 is allowable for these additional reasons as well.

G. Claim 25

The Office Action rejects claim 25 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 25 is allowable for at least the reason that *Aslanis* do not disclose, teach, or suggest at least an apparatus wherein a ***phase locked loop*** is used to accept an error signal to adjust the sampling time of the ADC. *Aslanis* does not disclose a PLL for adjusting the sampling rate of the ADC, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to adjust the sampling rate. Notwithstanding, the undersigned

has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach or suggest, either implicitly or explicitly, all the elements of claim 25 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 25 is allowable for these additional reasons as well.

H. Claim 28

The Office Action rejects claim 28 under 35 U.S.C. §103(a) as allegedly unpatentable over Aslanis *et al.* For the reasons set forth below, Applicants respectfully traverse the rejection.

For a proper rejection of a claim under 35 U.S.C. §103, the cited reference must disclose, teach, or suggest all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical.*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Applicants respectfully submit that independent claim 28 is allowable for at least the reason that *Aslanis* do not disclose, teach, or suggest at least an apparatus wherein a ***phase locked loop*** is used to accept an error signal to adjust the sampling time of the ADC. *Aslanis* does not disclose a PLL for adjusting the sampling rate of the ADC, but only a phase detector without any control loop mechanism. There is a control loop in *Aslanis* which includes an ADC, a TEQ, a buffer, an FFT, an FEQ and decoder, a phase comparator, control loop filters, and a voltage controlled oscillator. This is not a phase locked loop as disclosed in the present application, nor is there any impetus to use a PLL to adjust the sampling rate. Notwithstanding, the undersigned has reviewed the entirety of the *Aslanis* patent and has failed to identify any such teaching anywhere within this reference.

As shown above, the cited reference does not disclose, teach or suggest, either implicitly or explicitly, all the elements of claim 28 and, therefore, the rejection should be withdrawn. Additionally and notwithstanding the analysis hereinabove, claim 28 is allowable for these additional reasons as well.

VI. Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims. Other statements not explicitly addressed herein are not admitted.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-30 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,

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